Introduction

1.1 Overview

The following table contains the list of all known bugs in the PCI-DDC chip. They are sorted in the order they have been dectected. Some of them are even not detectable (1, 4, 6). Software workaround exist for all major bugs.

Mask#	Ref	Severity	workaround	Description
1	1	undetectable	not required	floating bulk in pad buffer
			Will not be corrected	
1	2	minor	not required	synchronous reset of the PCI signals
			Will not be corrected	
1	3	minor	hardware	synchronous reset of the RCUBE
			Will not be corrected	
1	4	undetectable	not required	FIFO status register
			Will not be corrected	
1	5	minor	software	no PCI vendor ID
			Will not be corrected	
1	6	undetectable	not required	IRDY signal
			Will not be corrected	
1	7	major	software	page descriptor ignored
			layout corrected	
1	8	major	software	receiving/configuration read conflict
			LAYOUT NOT CORRECTED	
1	9	major	software	bad data CRC checking
			layout corrected	
1	10	major	software	double writting of same word at consecutive addresses
			LAYOUT NOT CORRECTED	
1	11	minor	not required	Premature terminaison of memory write transaction
			layout corrected	
1	12	major	software	memory read transaction can never end
			layout corrected	
1	13	major	software	receiving a misaligned page
			LAYOUT NOT CORRECTED	
1	14	major	software	sending a misaligned page
			LAYOUT CORRECTION IN PROGRESS	
1	15	minor	software	message receive temporary blocked
			Will not be corrected	
1	16	major	software	no short message
			layout corrected for TX, LAYOUT NOT CORRECTED FOR RX	
1	17	minor	software	bad register addresses for LMI pointers
			Will not be corrected	
1	18	minor	software	LMI overflow acknowledge
			Will not be corrected	
1	19	minor	software	LMI overflow does not stop the reception
			Will not be corrected	
1	20	minor	software	message received counter frozen
			LAYOUT NOT CORRECTED	

1.2 Related Documents

Here is the list of documents, related to PCI-DDC, RCube, and the IEEE 1355 Standard.

PCIDDC_PB PCIDDC Product Brief
Single page document on PCIDDC Features.

PCIDDC_DS PCIDDC Data Sheet
This document.

PCIDDC_UM PCIDDC User Manual
Behavioral description of PCIDDC.

PCIDDC_CE PCIDDC Chip Errata
List of known bugs of PCIDDC.

RCUBE_PB RCube Product Brief
Single page document on the RCube router features.

RCUBE_DS RCube Data Sheet
Electrical and physical description of RCube.

RCUBE_UM RCube User Manual
Behavioral description of RCube.

IEEE1355 IEEE 1355 Standard
Specification document of the IEEE 1355 Standard.

PCI PCI Specification 2.1
Specification document of the PCI Standard.

1.3 Support

Feel free to contact MPC-SIG for any further information: **mpc@mpc.lip6.fr**

Bug description

2.1 Floating bulk in I/O buffer

The NWELL is floating in all I/O buffers.

Severity : undetectable

Workaround: not required

Status : not corrected

2.2 Synchronous reset of the PCI signals

The PCI signals (i.e. TRDY#, IRDY#, FRAME#, DEVSEL#, STOP# and also AD, C/BE#, PAR) should be asynchronously tri-stated, as soon as the RST# signal is asserted. They are not, the RST# signal effect is delayed till a clock edge appears. A conflict might occur between PCI-DDC and another PCI component during a short time, if this one does not respect this rule neither.

Severity : minor

The conflict time is rather short, i.e. few micro-seconds in the worst case. It depends actually of the time for the clock signal to appear after a reset signal. We did not notice any trouble during our tests.

Workaround : not required

Status : not corrected

2.3 Synchronous reset of the RCUBE

PCI-DDC drives a signal dedicated to the RCUBE reset, i.e. R3RESET. This signal is not asserted until a PCI CLK signal edge appears.

Severity : minor

RCUBE requires for its reset signal to be active at the power-on time in order to prevent internal short circuits. Actually, we did not notice trouble for the RCUBE chip.

Bug description
IRDY signal is held one cycle too long

Workaround : hardware

It is possible to add an external AND gate between the PCI-DDC R3RESET signal and the PCI RST# signal, in order that the RCUBE reset signal remains active until the PCI CLK signal edge appears.

Status : not corrected

2.4 FIFO status register

The status flags are undefined after a reset until a read or a write. It is not detectable since PCI-DDC always reads or writes the FIFOs before using the flags.

Severity : undetectable

Workaround : not required

Status : not corrected

2.5 No PCI vendor ID

The PCI-DDC Vendor ID is 0x0000. The device ID is 0x0000. This makes PCI-DDC not full PCI compliant. Note that this ID number value can create trouble for the OS.

Severity : minor

Workaround : maybe required, depending on the OS

Status : corrected by metal patch

2.6 IRDY signal is held one cycle too long

When PCI-DDC performs a memory read, and decides to close the transaction because its internal Tx-FIFO is full, the IRDY signal is held one extra cycle.

```
             PCI-DDC devices to close the transaction
                |    The target stops to send data
                |      |     PCI-DDC have to desasert IRDY the cycle before
                V      V        V
            |   ____|_______|________
FRAME#  ____|__/    |       |
            |       |       |   _____
IRDY#   ____|_______|_______|__/
            |       |   ____|________
TRDY#   ____|_______|__/    |
            |       |   ____|________
DEVSEL# ____|_______|__/    |
            |       |       |
                     <----->
                     bad cycle
```

Bug description
Double writting of same word at consecutive addresses

Severity : undetectable

This behaviour does not disturb the PCI-bus, since the only consequence is to delay the bus release. The bus just becomes idle one cycle later it should do.

Workaround : not required

Status : not corrected

2.7 Page descriptors ignored

PCI-DDC may ignore page descriptors.

Severity : major

Workaround : software

PCI-DDC must not have more than one page to send at the same time. The software can to put as many page descriptors as it wants in the LPE, if they are given to PCI-DDC one by one. It means that the software must take in charge the LPE pointers management.

Status : corrected by metal patch

2.8 Receive/configuration read conflict

If a configuration read occurs in the middle of a packet receive, the packet is corrupted.

Severity : major

Workaround : software

The workaround depends on the bridge behaviour. The goal is to avoid that a configuration read occurs while a packet is being received. The packet size must be limited to 16 bytes. This can be obtained using the configuration register 0x48: The MPL field must be set to 4.

Status : corrected by metal patch

2.9 Bad data CRC checking

An error may occurs in the CRC decoding while PCI-DDC is receiving a packet.

Severity : major

Workaround : software

The way to fix that bug is to limit the packet length to 16 bytes. (see PCI-DDC register 0x48).

Status : corrected by metal patch

2.10 Double writting of same word at consecutive addresses

If the network throughput is lower than the PCI bus throughput, it can happen bad configurations on the PCI bus where PCI-DDC writes the same data twice at consecutive addresses.

Bug description
Message receive temporary blocked

Severity : major

Workaround : software

It is required to limit the packet length to 16 bytes.

Status : corrected by metal patch

2.11 Overtaking of the legal wait-state number

PCI-DDC can generate more than 8 wait-states until the normal latency timer termination.

Severity : minor

Workaround : not required

Status : corrected by metal patch

2.12 Memory read transaction can never end

When a target disconnect occurs while the Tx-FIFO is full, PCI-DDC causes a PCI bus dead lock.

Severity : major

Workaround : software

Packet length must not be longer than 192 words (see PCI-DDC register 0x48).

Status : corrected by metal patch

2.13 Receiving a misaligned page

When PCI-DDC receives a misaligned packet and the target inserts wait-state, the byte enable (C/BE# PCI signals) are corrupted.

Severity : major

Workaround : software

Do not use misaligned messages longer than a word.

Status : corrected by metal patch

2.14 Sending a misaligned page

If the target inserts wait-states while PCI-DDC reads a misaligned page, a data may appear twice in the sent packet.

Severity : major

Workaround : software

Do not use misaligned messages longer than one word.

Bug description
LMI overflow does not stop reception.

Status : corrected by metal patch

2.15 Message receive temporary blocked

A page descriptor with a null page length (=0) may freeze the reception for one second.

Severity : minor

Workaround : software

Status : not corrected

2.16 No short messages

The short message mechanism does not work properly, consequently, the composed messages neither.

Severity : major

Workaround : software

Do not use short or composed messages.

Status : corrected by metal patch

2.17 Bad register addresses for LMI pointers

The PCI-DDC LMI_NEW register must be read at address 0x68 and written at address 0x64. The PCI-DDC LMI_CUR register must be read at address 0x64 and written at address 0x68.

Severity : minor

Workaround : software

Be carefull writing the software driver.

Status : documentation update

2.18 LMI overflow acknowledge

The LMI overflow error bit is acknowledge by writing 1 in the bit 13 of the PCI-DDC register 0x40 instead of bit 12. This causes both the LMI overflow and illegal LRM access errors to be acknowledged.

Severity : minor

Workaround : software

Be carefull when using these registers.

Status : corrected by metal patch

2.19 LMI overflow does not stop reception.

If the LMI overflow error mask is not set, PCIDDC does not freeze the reception when a LMI overflow occurs.

Severity : minor

Workaround : software

The LMI overflow mask must be set.

Status : documentation update

2.20 Message received counter frozen

If the message received mask is not set, the message received counter is frozen.

Severity : minor

Workaround : software

The mask interrupt must be set.

Status : corrected by metal patch